METHODS AND APPARATUS FOR GENERATING TEST INSTRUCTION SEQUENCES

Abstract of the Disclosure

Methods and apparatus are provided for automatically generating instruction sequences for verifying the operation of a processor, such as a central processing unit, a processor core, a graphics accelerator, or a digital signal processor. The instruction sequences can also be used to verify the operation of tools associated with implementing a processor. Test parameters are used to combine test fragments to generate test instructions. Check instructions are also provided to immediately identify faults encountered during operation.